Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in this application—including presently amended claims 5, 13, and 19.

Listing of Claims:

Claims 1-4 (Cancelled).

Claim 5 (Currently Amended): ~~The method of claim 4, in which the implanting further comprises~~ A method of fabricating a thyristor memory, comprising:

forming sidewalls in a layer of dielectric over a layer of semiconductor material to define a trench and expose a region of the semiconductor material through the opening of the trench;

forming conductive material on at least portions of the dielectric and in the trench;

patterning the conductive material to define first and second shoulders extending outwardly from the trench over regions of the dielectric outside the trench;

the patterning to comprise forming the first shoulder as an overhang extending laterally outward from the trench over regions of the layer of semiconductor material for the thyristor;

etching exposed regions of the layer of dielectric to form an implant mask while using the conductive material with the first and second shoulders as an etch mask;

implanting regions of the layer of semiconductor material; and

using the implant mask to align placement of dopant during at least a portion of the implanting;

in which the implanting comprises:

performing a first implant of first conductivity type dopant and penetrating with the dopant of the first conductivity type regions of the layer of semiconductor material beneath an edge of the implant mask to form a base region to the thyristor, with at least a portion thereof beneath the first shoulder; and

performing a second implant of second conductivity type dopant aligned with the implant mask and forming an anode/cathode-emitter.

Claim 6 (Original): The method of claim 5, in which the forming the trench comprises:

patterning first sacrificial material to cover a portion of the layer of semiconductor material to be associated with the trench;

layering dielectric over the semiconductor material and the patterned first sacrificial material;

planarizing at least one of the dielectric and the patterned first sacrificial material to form substantially equivalent heights therefor; and

after the planarizing, removing the patterned first sacrificial material to expose sidewalls of the dielectric and define the trench at least in part by the exposed sidewalls.

Claim 7 (Original): The method of claim 6, in which the forming the trench further comprises forming spacers of second dielectric against the sidewalls of the first dielectric, the spacers to narrow a width for the trench.

Claim 8 (Original): The method of claim 7, further comprising:

etching a portion of the semiconductor material exposed at a floor of the trench; and

recessing the floor of the trench relative to a plane defined by a surface of the semiconductor material outside the trench.

Claim 9 (Original): The method of claim 7, further comprising, before forming the conductive material, forming gate oxide over the exposed regions of the semiconductor material.

Claim 10 (Original): The method of claim 7, in which the etching the exposed regions of the dielectric comprises:

anisotropically etching the dielectric using the patterned conductive material as an etch mask; and

stopping the anisotropic etching after exposing a surface region of the semiconductor material.

Claim 11 (Original): The method of claim 10, further comprising:

removing material of the dielectric beneath the second shoulder; and

leaving at least a portion of the dielectric beneath the first shoulder.

Claim 12 (Original): The method of claim 11, in which the removing the material of the dielectric comprises:

isotropically etching the dielectric until exposing at least a portion of the spacer beneath the second shoulder; and

selectively etching the material of the dielectric using an etchant more favorable to etching the dielectric than either one of the semiconductor material and the second dielectric of the spacer.

Claim 13 (Currently Amended): The method of 12, in which:

the first implanting comprises using an acute angle of incidence for the first conductivity type dopant;

the second implanting comprises using a substantially orthogonal angel of incidence for the second conductivity type dopant; and

the first and the second implantings define a width for the base region that is less than the lateral extent of the first shoulder.

Claim 14 (Original): The method of claim 12, further comprising:

forming source, drain and body regions for an access transistor in the layer of semiconductor material;

forming a second emitter to the thyristor of first conductivity type in the layer of semiconductor material at a side of the conductive material opposite the first emitter; and

forming the second emitter in common with one of the source and drain regions of the access transistor.

Claim 15 (Original): The method of claim 14, in which the forming the second emitter and the forming the first base region define therebetween a second base region for the thyristor in the layer of semiconductor material, the second base region disposed in the layer of semiconductor material beneath the floor of the trench and between lateral edges of the respective first base and second emitter regions.

Claim 16 (Original): The method of claim 5, further comprising:

siliciding exposed regions of the layer of semiconductor material; and

using the implant mask during the siliciding to protect masked regions of the layer of semiconductor material.

Claim 17 (Original): The method of claim 16, further comprising:

implanting carrier lifetime adjustment species to affect leakage characteristics of the first emitter region; and

using the implant mask during the implanting of the carrier lifetime adjustment species to define an extent therefore.

Claim 18 (Original): The method of claim 16, in which the siliciding further comprises siliciding-exposed surface regions of the conductive material including exposed surface regions of the patterned first and second shoulders.

Claim 19 (Currently Amended): The method of claim 5, further comprising:

forming a layer of silicon over an insulator as the layer of semiconductor material ~~over an insulator~~;

the first implanting comprises penetrating a full-depth of the layer of silicon with the dopant of the first conductivity type; and

the second implanting comprises penetrating at least a partial depth of the layer of silicon with the dopant of the second conductivity type.

Claims 20-101 (cancelled as previously withdrawn).